IMPROVING THE EFFICIENCY OF FAULT SIMULATION BY LOGIC BACKTRACING

Abstract of the Disclosure

A method for improving the efficiency of fault simulation using logic fault backtracing is described. With existing fault tracing methods, it is a common occurrence that too many faults are identified as potential faults to be processed by fault simulation. The method of the invention improves the fault-simulation efficiency by explicitly processing only those faults that are identified by logic fault tracing as potential faults. The present invention also reduces the storage usage with concurrent fault simulations. The inventive method includes: a) performing a fault-free circuit simulation on a circuit having at least one fault to be tested by fault simulation using one or plural tests, each of the tests including at least one input test vector; b) based on the fault-free circuit simulation, identifying which faults in the logic circuit are potentially tested by the test; c) performing the fault simulation on all remaining faults that were identified as potentially tested by the test; and d) repeating the previous steps for each of the tests.